REMARKS

Status of Claims

Applicant respectfully requests reconsideration and allowance of all of the claims of the Application. The status of the claims is as follows:

- Claims 1-3 and 5-12 and 16-22 are currently pending;
- Claims 13-15 are canceled herein;
- No claims are withdrawn herein;
- Claims 1, 6, 11, 12 and 16 are amended herein;
- New claims 21-22 are added herein; and
- Claims 1, 11 and 16 are independent.

Support for the amendments to the claims is found in the specification, for example, at least at page 19, line 19, through page 20, line 10 of Applicant's original specification filed on February 2, 2004.

Allowable Subject Matter

Dependent claims 15 and 19 were objected to as depending from a rejected base claim. The Examiner has indicated that these claims would be allowable if rewritten in independent form including all of the features of the base claims from which they depend and any intervening claims. Applicant thanks the Examiner for this indication of allowable subject matter.

Claim 15 has been incorporated into base claim 11, and thereby rewritten herein in independent form. There were no intervening claims. Accordingly, Applicant respectfully submits that independent claim 11 is now in condition for allowance. Claim 12, which depends from allowable claim 11, has been amended. Applicant respectfully submits that claim 12 is also in condition for allowance, at least because claim 12 depends from allowable base claim 11. Further, dependent claims 13-15, which depended from claim 11, have been canceled.

Cited Documents

The following documents have been applied to reject one or more claims of the Application:

- **Parry**: Parry et al., U.S. Patent No. 6,535,920
- **Lortz**: Lortz, U.S. Patent No. 7,047,554
- **DeLeeuw**: DeLeeuw, U.S. Patent No. 6,088,018

Anticipation Rejections of Claims 1-3, 5-14, 16-18, and 20

Claims 1-3, 5-14, 16-18 and 20 stand rejected under 35 USC § 102(e) as allegedly being anticipated by Parry. Claims 1-3, 5-14, 16-18 and 20 stand rejected under 35 USC § 102(e) as allegedly being anticipated by Lortz. Claims 1-3, 5-14, 16-18 and 20 stand rejected under 35 USC § 102(e) as allegedly being anticipated by DeLeeuw. Applicant respectfully traverses these rejections, and asks the Examiner to reconsider and withdraw the rejections for the following reasons.

Independent Claims 1 and 16

Applicant submits that Parry, Lortz and/or DeLeeuw do not anticipate, and the combination of Parry, Lortz and/or DeLeeuw with each other and/or the other art of record does not teach or suggest at least the following elements, as recited in independent claim 1 (with emphasis added):

> ...a media source of media content;
>
> a matrix switch having a plurality of matrix switch inputs and a plurality of matrix switch outputs, wherein the matrix switch dynamically couples particular ones of the matrix switch inputs to particular ones of the matrix switch outputs based, at least in part, on a matrix switch programming grid;
>
> a software object, coupling the media source to one or more of a plurality of processing chains, to satisfy multiple, non-combinable requests to the media source for the media content received from the matrix switch, wherein the non-combinable requests for media content include one or more of: requests where a source time of the requested media content do not align, requests where a project time of the requests do not align, or requests where the requested media content is to be processed differently so as to require a separate processing chain, ***wherein a first one of the plurality of processing chains is linked with a first matrix switch input of the plurality of inputs that is dynamically coupled to a first matrix switch output of the plurality of outputs, wherein the matrix switch is configured to share a buffer of the first matrix switch input with the first matrix switch output to which the first matrix switch input is dynamically coupled;***
>
> one or more processing units configured to implement the software object and the matrix switch; and
>
> a system memory configured to store the software object.

Parry describes a system for processing streaming information (e.g., col. 6, lines 26-27). At pages 2-3 of the Office Action, it is asserted that Parry anticipates Applicant's claim 1, citing col. 6 of Parry. However, Applicant respectfully notes that col. 6 of Parry describes the following:

FIG. 5 is a general block diagram illustrating a system 110 for processing streaming information. System 110 includes a delay filter 112 for temporarily storing streaming information received from a streaming information source 114. Delay filter 112 is further coupled to a rendering device or devices 116 to render streaming information upon request by the user. Also illustrated in FIG. 5 is an encoder 118 and a decoder 120. Although not required, encoder 118 and decoder 120 can improve system performance wherein encoder 118 receives streaming information source 114 and compresses the streaming information prior to transfer and storage in delay filter 112. Decoder 120 receives the streaming information temporarily stored in delay filter 112 in the compressed format and uncompresses the streaming information prior to transferring the streaming information to rendering device 116 (Parry, col. 6, lines 26-41).

At this point, it should be noted that system 110 can be operated in any of the computing environments described above, or similar computing environments. Those skilled in the art will appreciate that delay filter 112, rendering device 116, encoder 118 and decoder 120 can be implemented in hardware, software, or combinations thereof. In one embodiment by way of example, delay filter 112 is embodied in the operating system. Higher level application programs or other portions of the operating systems can access functions of delay filter 112 using application program interfaces (APIs) as is well known in the art (Parry, col. 6, lines 42-52).

In operation, streaming information source 114 provides an information stream to delay filter 112 (optionally through encoder 118). Generally, the streaming information comprises digital data representing one or more channels of content information. For instance, streaming information source 114 can comprise an Intranet or the Internet available through the communication interfaces described above. Likewise, streaming information source 114 can comprise an analog or digital television tuner wherein separate audio, video and data (e.g. closed captioning) information streams comprise a single channel. Other sources of streaming information include, but are not limited to, audio tuners, satellite receivers and the like (Parry, col. 6, lines 53-65).

From a review of the foregoing reproduced portions of Parry, and the remainder of Parry, Applicant has been unable to discern any portion of Parry that discloses ***wherein a first one of the plurality of processing chains is linked with a***

first matrix switch input of the plurality of inputs that is dynamically coupled to a first matrix switch output of the plurality of outputs, wherein the matrix switch is configured to share a buffer of the first matrix switch input with the first matrix switch output to which the first matrix switch input is dynamically coupled, as recited in Applicant's claim 1. For example, Applicant's specification describes the following:

> According to one implementation, for each input 402 and output 404, matrix switch 308 attempts to be the allocator, or manager of the buffer associated with the I/O(s) shared with adjacent filters. One reason is to ensure that all of the buffers are of the same size and share common attributes so that a buffer associated with any input 402 may be shared with any output 404, thereby reducing the need to copy memory contents between individual buffers associated with such inputs/outputs (page 20, lines 1-7 of Applicant's original specification).

On the other hand, Parry merely describes "a delay filter 112 for temporarily storing streaming information received from a streaming information source 114" (Parry, col. 6, lines 28-29). Parry further describes that "Delay filter 112 is further coupled to a rendering device or devices 116 to render streaming information upon request by the user" (Parry, col. 6, lines 29-32). Thus, rather than disclosing ***wherein a first one of the plurality of processing chains is linked with a first matrix switch input of the plurality of inputs that is dynamically coupled to a first matrix switch output of the plurality of outputs, wherein the matrix switch is configured to share a buffer of the first matrix switch input with the first matrix switch output to which the first matrix switch input is dynamically coupled***, as recited in Applicant's claim 1, Parry merely describes that "streaming information source 114 provides an information stream to delay filter 112 (optionally through encoder 118)" (e.g., Parry, col. 6, lines 53-55).

Thus, Applicant respectfully submits that amended claim 1 is allowable over Parry for at least this aspect.

Lortz also fails to disclose at least the above-emphasized clause of Applicant's claim 1. For example, Lortz describes controlling at least two audio/video (A/V) devices to render a desired content in which a filter graph is constructed for at least two A/V devices as a function of a connection topology of the at least two A/V devices and the desired content (e.g., Lortz, col. 2, line 66, through col. 3, line 3).

At page 8 of the Office Action, it is asserted that Lortz anticipates Applicant's claim 1, citing col. 3 of Lortz. However, Applicant respectfully notes that col. 3 of Lortz describes the following:

> FIG. 1 shows an example of a system according to the present invention, which includes a processor 10 coupled to a storage device 20, a command transmission means 30 for controlling at least two A/V devices 40, 50, and an input device 35. Command transmission device 30 may include a data communication cable (e.g., serial cable, parallel cable), an I/R (infrared) transmitter, an RF (radio frequency) transmitter, or comparable means. The number and type of command transmission device 30 may vary for each implementation depending on the type of A/V devices that are controlled by the system. For example, if the A/V devices include an IEEE 1394-compliant device 40 such as, for example, a DVD (digital video disk) player, command transmission device 30 may include a serial cable. If the A/V devices also include an analog device 50 such as, for example, an analog television or stereo, command transmission device 30 may also include an I/R transmitter or an RF transmitter. Using this configuration, processor 10 is capable of individually controlling A/V devices 40, 50. Since these types of computer-based control systems are known to those of skill in the art, they will not be discussed in further detail herein (Lortz, col. 3, lines 28-49).
>
> Input device 35 receives commands from the user. Input device 35 may include, for example, a keyboard, a mouse, a microphone, etc. The keyboard and mouse may be remote devices that communicate with processor 10 via, for example, infrared or radio frequency signals. A microphone may be used

> with conventional speech recognition algorithms or natural language processing to determine the user input (Lortz, col. 3, lines 50-57).
>
> Storage device 20 may include a device filters table 60, which may have a structure as shown in FIG. 2A. Each entry in device filters table 60 includes specific characteristics of a corresponding A/V device. For example, each device filter may include fields for its designated name, pins (either input or output, or both), media type, supported functions, and location of the corresponding A/V device. The name may be used to identify the individual A/V device (Lortz, col. 3, lines 58-65).

From a review of the foregoing reproduced portions of Lortz, and the remainder of Lortz, Applicant has been unable to discern any portion of Lortz that discloses ***wherein a first one of the plurality of processing chains is linked with a first matrix switch input of the plurality of inputs that is dynamically coupled to a first matrix switch output of the plurality of outputs, wherein the matrix switch is configured to share a buffer of the first matrix switch input with the first matrix switch output to which the first matrix switch input is dynamically coupled***, as recited in Applicant's claim 1. Instead, Lortz merely describes that "each device filter may include fields for its designated name, pins (either input or output, or both), media type, supported functions, and location of the corresponding A/V device" (Lortz, col. 3, lines 61-64). Thus, Applicant respectfully submits that amended claim 1 is allowable over Lortz for at least the elements of the above-emphasized clause.

In addition, DeLeeuw also fails to disclose at least the above-emphasized clause of Applicant's claim 1. For example, DeLeeuw describes capturing an image of a user and rendering the image in a transparent manner to a display (e.g., DeLeeuw, col. 4, lines 10-13).

At page 13 of the Office Action, it is asserted that DeLeeuw anticipates Applicant's claim 1, citing col. 4 of DeLeeuw. However, Applicant respectfully notes that col. 4 of DeLeeuw describes the following:

> An underlying capability of some embodiments of the present invention is a method of providing a transparent layer of display data signals (such as video data signals communicated by a video camera, for example) over the top of another layer of display data signals on a computer display so that the user may see both layers clearly and substantially simultaneously. This capability will be described first for general use and further below for use with an input detection method of some embodiments of the present invention. The capability to display transparent windows doubles, in essence, the maximum screen area available on a display for use by application programs. One embodiment is a method for producing transparent computer graphics layers by interleaving (or alternating in a pattern) the pixels from one video frame buffer with the pixels from another video frame buffer. In this embodiment, selected pixels from a first frame buffer are mixed by color averaging with corresponding pixels from a second frame buffer to reduce the "checkerboard" effect created by the use of spatial multiplexing alone. Additionally, because the degree of interleaving is adjustable and the color averaging may be weighted, the degree of transparency of the displayed images may be controlled (DeLeeuw, col. 4, lines 16-38).
>
> In this embodiment, an output frame buffer used by operating system software is not affected by provision of the transparency feature and the operating system is unaware of the transparency operations. Hence, the transparency effect provided by embodiments of the present invention does not require modifications to application programs for transparency to work over them. Furthermore, input operations to application program and operating system windows are not affected by transparent foreground effects (DeLeeuw, col. 4, lines 39-47).
>
> An embodiment of the present invention operates by combining at least two frame buffers of computer graphics output data or video data in the form of electrical signals. The pixels of the output, or visible, frame buffer are created by spatially interleaving the contents of two input frame buffers. The interleaving in this embodiment is accomplished by combining pixels of one frame buffer with those of the other frame buffer. This results in the visual illusion of two displays of images layered one on another.

> As the pixels are being interleaved, the pixels of the first frame buffer are color averaged with the pixels of the second frame buffer that they are about to replace. Color averaging is performed on the pixels of one frame buffer by averaging them with the corresponding pixels of the other frame buffer prior to, or during, interleaving them into the output frame buffer. The result comprises multiple overlapping images being substantially simultaneously visible on a display such as a computer monitor, for example (DeLeeuw, col. 4, lines 48-65).

From a review of the foregoing reproduced portions of DeLeeuw, and the remainder of DeLeeuw, Applicant has been unable to discern any portion of DeLeeuw that discloses ***wherein a first one of the plurality of processing chains is linked with a first matrix switch input of the plurality of inputs that is dynamically coupled to a first matrix switch output of the plurality of outputs, wherein the matrix switch is configured to share a buffer of the first matrix switch input with the first matrix switch output to which the first matrix switch input is dynamically coupled***, as recited in Applicant's claim 1. Instead, DeLeeuw merely describes that "selected pixels from a first frame buffer are mixed by color averaging with corresponding pixels from a second frame buffer to reduce the "checkerboard" effect created by the use of spatial multiplexing alone" (DeLeeuw, col. 4, lines 31-35). DeLeeuw further describes that "Color averaging is performed on the pixels of one frame buffer by averaging them with the corresponding pixels of the other frame buffer prior to, or during, interleaving them into the output frame buffer" (DeLeeuw, col. 4, lines 59-63). However, Applicant has been unable to locate any disclosure in DeLeeuw of ***wherein a first one of the plurality of processing chains is linked with a first matrix switch input of the plurality of inputs that is dynamically coupled to a first matrix switch output of the plurality of outputs, wherein the matrix switch is***

configured to share a buffer of the first matrix switch input with the first matrix switch output to which the first matrix switch input is dynamically coupled, as recited in Applicant's claim 1. Thus, Applicant respectfully submits that amended claim 1 is allowable over DeLeeuw for at least the elements of the above-emphasized clause.

Applicant has shown above by direct quotation that the cited portions of Parry, Lortz and/or DeLeeuw are very different on their faces from the above-emphasized clause of Applicant's claim 1. Therefore, Applicant respectfully submits that Parry, Lortz and/or DeLeeuw do not anticipate Applicant's claim 1 because each and every element of Applicant's claim 1 is not present in Parry, Lortz and/or DeLeeuw. Furthermore, Applicant respectfully submits that the combination of Parry, Lortz, DeLeeuw with each other, and/or the other art of record also does not teach or suggest Applicant's amended claim 1.

In view of the foregoing, Applicant respectfully submits that claim 1 is allowable over Parry, Lortz and/or DeLeeuw and/or the other art of record, and is in condition for allowance. Applicant respectfully requests that the Examiner withdraw the rejection of claim 1. Accordingly, for at least the foregoing reasons, Applicant respectfully asks the Examiner to hold independent claim 1 allowable and to issue a Notice of Allowance of same.

Independent claim 16, as amended, includes language similar to that discussed above with reference to claim 1, and is allowable under a similar rationale. Applicant respectfully requests that the Examiner withdraw the rejection of claim 16. Further, for at least the foregoing reasons, Applicant respectfully asks the Examiner to hold independent claim 16 allowable and to issue a Notice of Allowance of same.

Dependent Claims

In addition to its own merits, each dependent claim is allowable for the same reasons that its base claim is allowable. Applicant requests that the Examiner withdraw the rejection of each dependent claim where its base claim is allowable.

Conclusion

Applicant submits that all pending claims are in condition for allowance. Applicant respectfully requests reconsideration and prompt issuance of the application. If any issues remain that prevent issuance of this application, the Examiner is urged to contact the undersigned representative for the Applicant before issuing a subsequent Action.

Respectfully Submitted,

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